AKM

AK4309A

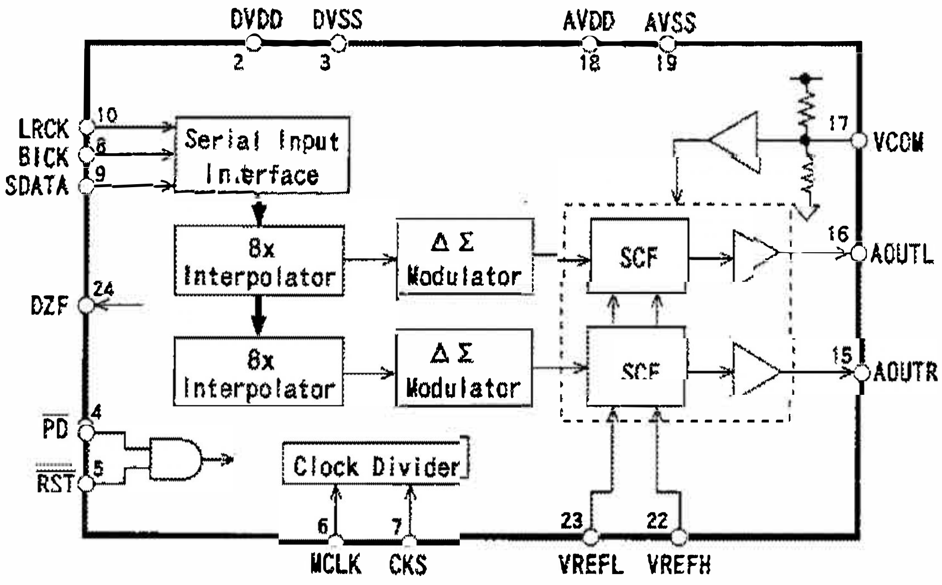
16Bit Stereo Δ Σ DAC for Multimedia

General Description

The AK4309A is a 1bit stereo DAC for multimedia audio systems. A 1bit DAC can achieve monotonicity and low distortion with no adjustment and is superior to traditional R-2R ladder based DACs. In the AK4309A, the loss of accuracy from clock jitter is also improved by using SCF techniques for on-chip post filter. The AK4309A includes continuous time filter with single end output and does not need any external parts. The master clock can be either 256fs or 384fs, supporting various audio environment.

Features

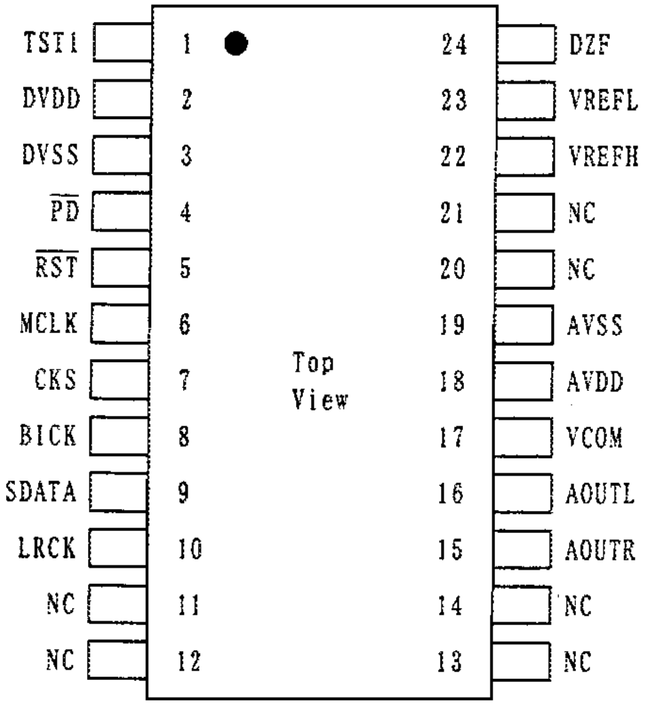
- ☐ 1bit Δ Σ DAC
- ☐ Sampling Rate Ranging from 10kHz to 50kHz
- ☐ On chip Perfect filtering
  - ・ 8 times FIR Interpolator
  - ・ 2nd order SCF
  - ・ 2nd order CTF
  - ・ Total Response: ± 0.5dB at 20kHz
- ☐ On chip Buffer with Single End Output
- ☐ Master Clock: 256fs or 384fs
- ☐ High Tolerance to Clock Jitter
- ☐ TTL Level Digital Interface
- ☐ THD+N: -85dB
- ☐ Dynamic Range: 91dB
- ☐ Output Level: 3.4Vpp
- ☐ Power Supply: 5V ± 10%
- ☐ Low Power Dissipation: 80mW at 5V
- ☐ Small Package: 24pin SSOP
- ☐ Pin Compatible with AK4310/AK4309



■ Ordering Guide

AK4309A-VM	-10～+70℃	24pin SSOP (0.65mm pitch)
AKD4310	Evaluation Board (AK4309A's board is the same as AK4310's)	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	TST1	I	Test Pin (Pull-down pin) Must be left floating or tied to DGND.
2	DVDD	-	Digital Power Supply Pin
3	DVSS	-	Digital Ground Pin
4	$\overline{\text{PD}}$	I	Power-Down Pin When at "L", the AK4309A is in power-down mode and is held in reset. The AK4309A should always be reset upon power-up.
5	$\overline{\text{RST}}$	I	Reset Pin This pin has the same function as the $\overline{\text{PD}}$ pin. The $\overline{\text{PD}}$ pin and the $\overline{\text{RST}}$ pin are ANDed internally.
6	MCLK	I	Master Clock Input Pin An external CMOS clock should be input on this pin. The fs is selected by CKS pin.
7	CKS	I	Master Clock Select Pin "L": MCLK=256fs "H": MCLK=384fs
8	BICK	I	Serial Bit Input Clock Pin This clock is used to latch SDATA.
9	SDATA	I	Serial Data Input Pin 2's complement MSB-first data is input on this pin.
10	LRCK	I	L/R Clock Pin This input determines which channel is currently being input on the Serial Data Input pin, SDATA. "H": Lch, "L": Rch
15	AOUTR	O	Rch analog output pin
16	AOUTL	O	Lch analog output pin
17	VCOM	O	Common Voltage pin, AVDD/2 Normally connected to AVSS with a 0.1uF ceramic capacitor in parallel with a 10uF electrolytic cap.
18	AVDD	-	Analog Power Supply Pin
19	AVSS	-	Analog Ground Pin
22	VREFH	I	"H" Voltage Reference Input Pin The differential Voltage between VREFH and VREFL inputs set the analog output range. The VREFH pin is normally connected to AVDD and the VREFL pin is connected to AVSS. A 0.1uF ceramic capacitor should be as near to both pins.
23	VREFL	I	"L" Voltage Reference Input Pin
24	DZF	O	Zero Input Detect Pin When SDATA of both channels follow a total 8192 LRCK cycles with "0" input data, this pin goes "H".

* All pins except the above pins are NC pins. These pins are not bonded internally.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supplies: Analog (AVDD pin)	AVDD	-0.3	6.0	V
Digital (DVDD pin)	DVDD	-0.3	AVDD+0.3	V
Input Current, Any Pin Except Supplies	IIN	-	±10	mA
Input Voltage	VIND	-0.3	AVDD+0.3	V
Ambient Operating Temperature	Ta	-10	70	℃
Storage Temperature	Tstg	-65	150	℃

Note: 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supplies: Analog (AVDD pin)	AVDD	4.5	5.0	5.5	V
Digital (DVDD pin)	DVDD	4.5	5.0	AVDD	V
"H" Voltage Reference (Note 2)	VREFH	-	-	AVDD	V
"L" Voltage Reference	VREFL	AVSS	-	-	V
VREFH-VREFL	ΔVREF	3.0	-	AVDD	V

Notes: 1. All voltages with respect to ground.

2. Analog output voltage scales with the voltage of (VREFH-VREFL).
AOUT(typ. @0dB)=3.4Vpp*(VREFH-VREFL)/5。

ANALOG CHARACTERISTICS

(Ta=25℃; AVDD, DVDD=5.0V; VREFH=AVDD, VREFL=AVSS; fs=44.1kHz; Signal Frequency=1kHz; $R_L \geq 10k\Omega$; Measurement Bandwidth=10Hz～20kHz; unless otherwise specified)

Parameter	min	typ	max	Units
Dynamic Characteristics				
THD+N		-85	-79	dB
Dynamic Range (A-Weighted)	85	91		dB
S/N (A-Weighted)	85	91		dB
Interchannel Isolation	80	90		dB
DC Accuracy				
Interchannel Gain Mismatch		0.1	0.2	dB
Gain Drift	-	60	-	ppm/℃
Analog Output				
Output Voltage (Note 3)	3.23	3.4	3.57	Vpp
Load Resistance	10			kΩ
Load Capacitance (Note 4)			300	pF
Power Supplies				
Power Supply Current (Note 5)				
Normal Operation ($\overline{PD}$ and $\overline{RST}$="H")				
AVDD		13	19	mA
DVDD		3	5	mA
Power-Down-Mode ($\overline{PD}$ and $\overline{RST}$="L")				
AVDD+DVDD (Note 6)		10	50	uA
Power Dissipation				
Normal Operation		80	120	mW
Power-Down-Mode (Note 6)		50	250	uW
Power Supply Rejection		50		dB

Notes:3. Full-scale voltage(0dB). Output voltage scales with the voltage of (VREFH-VREFL). AOUT(typ. @0dB)=3.4Vpp*(VREFH-VREFL)/5.

4. A resistor(more than 200Ω) should be added in series between AOUT and capacitive load.

5. $\overline{PD}$ pin and the $\overline{RST}$ pin are ANDed internally.

6. Power Dissipation in the power-down mode applies with no external clocks applied (MCLK, BICK, LRCK held "H" or "L").

FILTER CHARACTERISTICS

(Ta=25℃ ; AVDD, DVDD=4.5～5.5V; fs=44.1kHz)

Parameter	Symbol	min	typ	max	Units
Digital Filter					
Passband ±0.2dB (Note 7)	PB	0		20.0	kHz
-6.0dB			22.05		kHz
Stopband (Note 7)	SB	24.3			kHz
Passband Ripple	PR			±0.05	dB
Stopband Attenuation	SA	41			dB
Digital Filter + Analog Filter					
Group Delay (Note 8)	GD		14.5		1/fs
Frequency Response 0～20.0kHz			±0.5		dB

Note: 7. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs (@-0.2dB), SB=0.5896*fs (@-41dB).

8. The calculating delay time which occurred by digital filtering. This time is from setting the 16bit data of both channels to input register to the output of analog signal.

DC CHARACTERISTICS

(Ta=25℃; AVDD, DVDD=4.5～5.5V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	2.2	-	-	V
Low-Level Input Voltage	VIL	-	-	0.6	V
High-Level Output Voltage Iout=-100uA	VOH	DVDD-0.5	-	-	V
Low-Level Output Voltage Iout=100uA	VOL	-	-	0.5	V
Input Leakage Current	Iin	-	-	±10	uA

SWITCHING CHARACTERISTICS

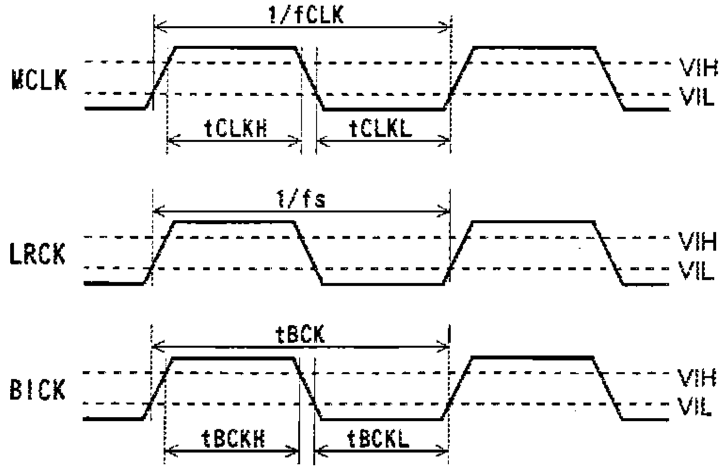
(Ta=25℃; AVDD, DVDD=4.5～5.5V; C_L=20pF)

Parameter	Symbol	min	typ	max	Unit
Master Clock Frequency					
256fs:	fCLK	2.56	11.2896	12.8	MHz
Pulse Width Low	tCLKL	28			ns
Pulse Width High	tCLKH	28			ns
384fs:	fCLK	3.84	16.9344	19.2	MHz
Pulse Width Low	tCLKL	23			ns
Pulse Width High	tCLKH	23			ns
LRCK Frequency (Note 9)	fs	10	44.1	50	kHz
Serial Interface Timing (Note 10)					
BICK Period	tBCK	312.5			ns
BICK Pulse Width Low	tBCKL	100			ns
Pulse Width High	tBCKH	100			ns
LRCK Edge to BICK Rising (Note 11)	tLRB	50			ns
BICK falling to LRCK Edge (Note 11)	tLRB	50			ns
SDATA Hold Time	tSDH	50			ns
SDATA Setup Time	tSDS	50			ns
Reset Timing					
$\overline{PD}$, $\overline{RST}$ Pulse Width (Note 12)	tRST	100			ns

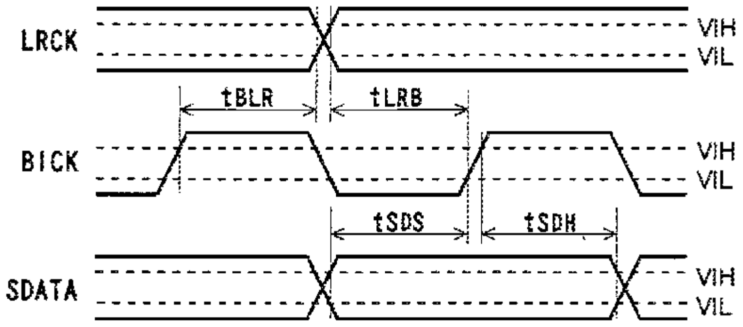
Notes: 9. If the duty of LRCK changes later than ±1/8 from 50%, the AK4309A is reset by the internal phase circuit automatically.

10. Refer to the operating overview section "Serial Data Interface".
11. BICK rising edge must not occur at the same time as LRCK edge.
12. The AK4309A can be reset by bringing $\overline{PD}$*$\overline{RST}$ "L" to "H" only upon power up.

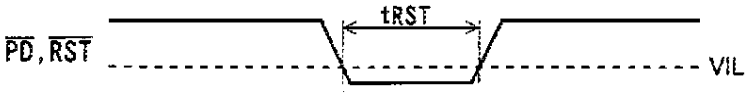
■ Timing Diagram



Clock Timing



Serial Interface Timing



Reset Timing

OPERATION OVERVIEW

■ System Clock Input

The external clocks which are required to operate the AK4309A are MCLK(256/384fs), LRCK(fs), BICK(32fs～). MCLK should be synchronized with LRCK but the phase is free of care. The frequency of MCLK is determined by the desired Input Word Rate(fs), and the setting of the Clock Select, CKS pin. Setting CKS "L" selects an MCLK frequency of 256fs while setting CKS "H" selects 384fs. When the 384fs is selected, the internal master clock becomes 256fs(=384fs*2/3). Table 1 illustrates standard audio word rates and corresponding frequencies used in the AK4309A.

As the AK4309A includes the phase detect circuit using LRCK, the AK4309A is reset automatically when the synchronization is out of phase by changing the clock frequencies. Therefore, the reset is not needed except only upon power-up. (Please refer to the "System Reset" section.)

All external clocks(MCLK, BICK, LRCK) should always be present whenever the AK4309A is in normal operation mode($\overline{PD}*\overline{RST}$="H"). If these clocks are not provided, the AK4309A may draw excess current and may not possibly operate properly because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4309A should be in the power-down mode($\overline{PD}*\overline{RST}$="L").

fs	MCLK		BICK(32fs)
	256fs	384fs	
32.0kHz	8.1920MHz	12.2880MHz	1.0240MHz
44.1kHz	11.2896MHz	16.9344MHz	1.4112MHz
48.0kHz	12.2880MHz	18.4320MHz	1.5360MHz

Table 1. Examples of System Clock

■ Serial Data Interface

The AK4309A has three serial input pins(SDATA, BICK, LRCK). Data bits are clocked into the AK4309A via SDATA pin and are latched by LRCK. The data format is MSB-first and 2's complement.

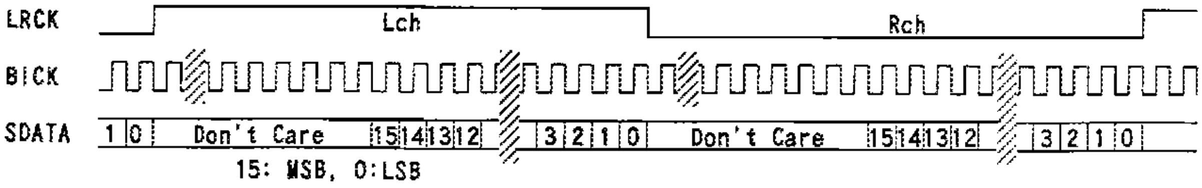


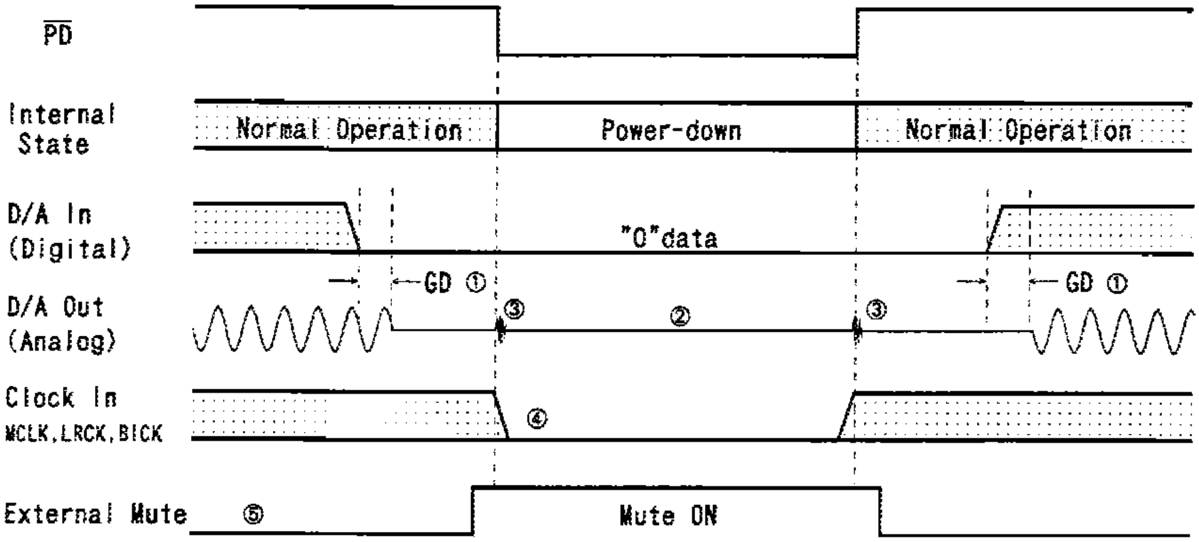
Figure 1. Data Input Format

■ Zero detection

When the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF goes to "H". DZF immediately goes "L" if input data are not zeros after going DZF "H".

■ Power-Down

The AK4309A is placed in the power-down mode by setting $\overline{\text{PD}}$ pin or $\overline{\text{RST}}$ pin "L". In the power-down mode, the analog outputs go floating.



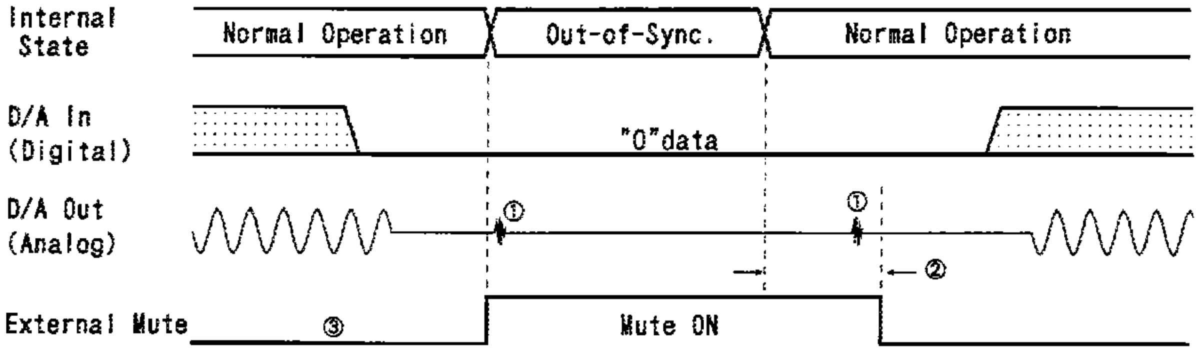
Notes:

①Analog output corresponding to digital input has the group delay(GD).
②Analog outputs are floating(Hi-Z) at the power-down mode.
③Click noise about -50dB occurs at the edges("↑ ↓") of $\overline{\text{PD}}$ signal.
④When the external clocks(MCLK, BICK, LRCK) are stopped, the AK4309A should be in the power-down mode.
⑤Please mute the analog output externally if the click noise(③) influences system application. The timing example is shown in this figure.

Figure 2. Power-down/up sequence example

■ System Reset

The AK4309A should be reset once by bringing $\overline{PD}$ or $\overline{RST}$ "L" upon power-up. The internal timing starts clocking by LRCK "↑" after exiting reset by MCLK. If the phase difference between LRCK and internal control signals is larger than +1/16~-1/16 of word period(1/fs), the synchronization of internal control signals with LRCK is done automatically at the first rising edge of LRCK. Since RAM address shifts during this synchronization, correct data would not be output until 14 sampled data are input even if the AK4309A returns to the normal operation. Refer to Figure 3.



When cycle ratio between LRCK and XTI can not be kept 1:256(1:384 at 384fs) by changing LRCK frequency etc., internal reset by out-of-synchronization may occur. Some noise about -50dB occurs at resetting and after returning to normal operation. This noise also occurs evenif "0" data is being input to the AK4309A.

①Click noise is output continuously when out-of-synchronization occurs continuously.
②Some noise occurs until 14*LRCK cycles after LRCK returns to normal condition.
③Please mute the analog output externally if there is a possibility of out of synchronization in the application. The timing example is shown in this figure.

Figure 3. Out-of-synchronization timing example

SYSTEM DESIGN

Figure 4 shows the system connection diagram. An evaluation board[AKD4310] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

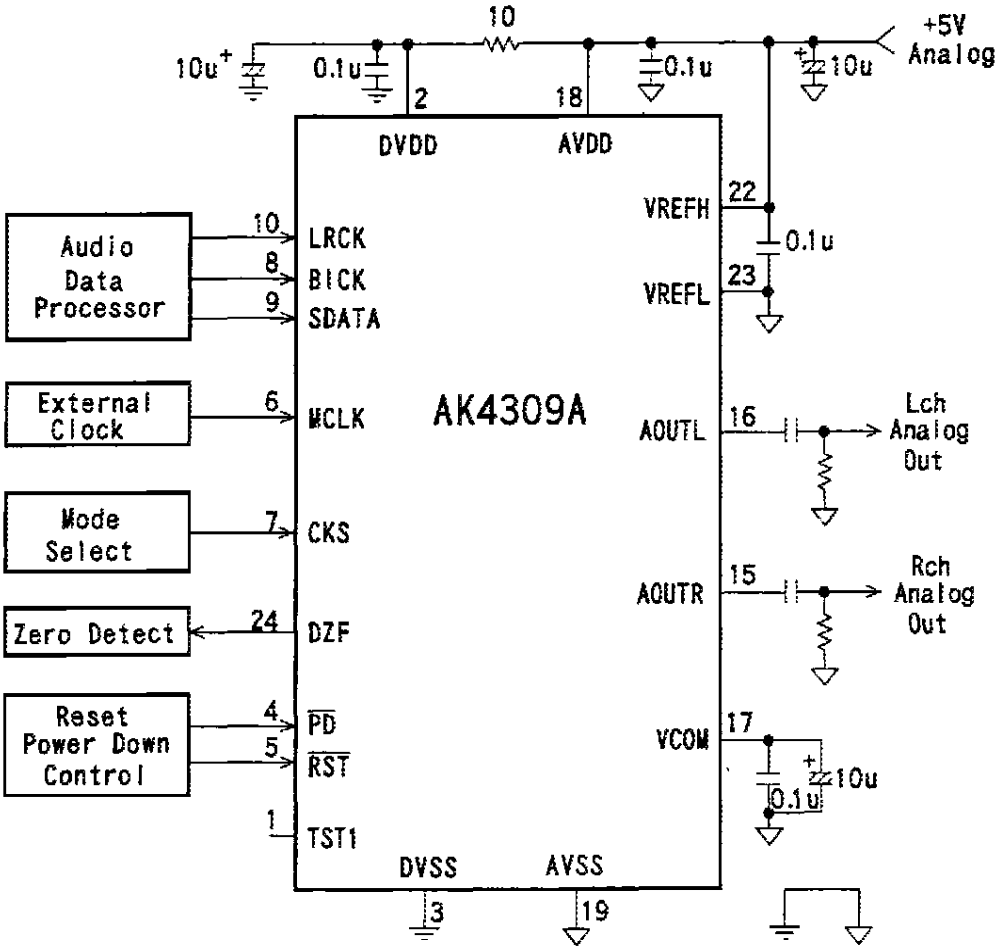


Figure 4. Typical Connection Diagram

Notes:

- LRCK=fs, BICK≧32fs, MCLK=256fs at CKS="L", MCLK=384fs at CKS="H".
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.

■ System design consideration

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD and DVDD, respectively. AVDD is supplied from analog supply in system and DVDD is supplied from AVDD via 10Ω resistor. Alternatively if AVDD and DVDD are supplied separately, AVDD and DVDD should be powered at the same time or AVDD should be powered earlier than DVDD. Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors for high frequency should be as near to the AK4309A device as possible, with the low value ceramic capacitor across VREFH and VREFL being the nearest.

2. Voltage reference

The differential Voltage between VREFH and VREFL set the analog output range. VREFH pin is normally connected to AVDD and VREFL pin is connected to AVSS. A 0.1uF ceramic capacitor should be as near to both pins. VCOM is a signal ground of this chip. An electrolytic capacitor less than 10uF in parallel with a 0.1uF ceramic capacitor attached to these pins eliminates the effects of high frequency noise. No load current may be drawn from VCOM pin. All signals, especially clocks, should be kept away from VREFH, VREFL and VCOM pins in order to avoid unwanted coupling into the AK4309A.

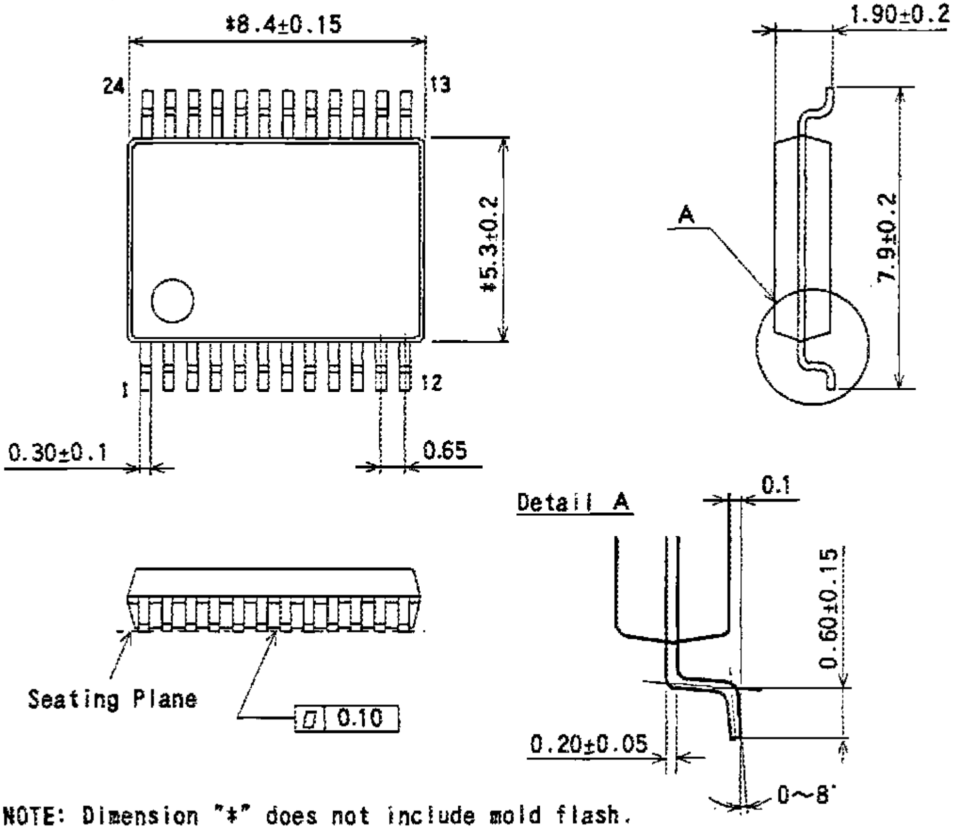
3. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The output signal range is typically 3.4Vpp. AC coupling capacitors of larger than 1uF are recommended. The internal switched-capacitor filter and continuous-time filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband. Therefore, any external filters are not required for typical application. The output voltage is a positive full scale for 7FFFH(@16bit) and a negative full scale for 8000H(@16bit). The ideal output is VCOM voltage for 0000H(@16bit).

DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have DC offsets of a few mV.

PACKAGE

● 24pin SSOP (Unit: mm)

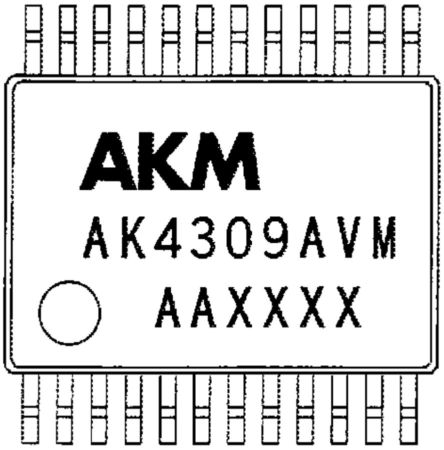


NOTE: Dimension "*" does not include mold flash.

■ Package & Lead frame material

Package molding compound :	Epoxy
Lead frame material :	Cu
Lead frame surface treatment:	Solder plate

MARKING



Contents of AAXXXX
AA : Lot#
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